93 - 03 - 29 OMB No. 0704-0188 (See MIL-STD-480 for instructions) This revision described below has been authorized for the document listed Public reporting burden for this collection is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Information and Regulatory Affairs, Office of Management and Budget, Washington, DC 20503. 2. CAGE CODE 3. NOR NO. 1. ORIGINATOR NAME AND ADDRESS 67268 5962-R113-93 Defense Electronics Supply Center Dayton, Ohio 45444-5277 4. CAGE CODE 5. DOCUMENT NO. 67268 5962-88739 6. TITLE OF DOCUMENT 7. REVISION LETTER MICROCIRCUITS, DIGITAL, CMOS, 8 X 8 MULTIPLIER, MONOLITHIC (Current) C (New) D SILICON 8. ECP NO. 9. CONFIGURATION ITEM (OR SYSTEM) TO WHICH ECP APPLIES 10. DESCRIPTION OF REVISION Sheet 1: Revisions ltr column; add "D". Revisions description column; add "Changes in accordance with NOR 5962-R113-93". Revisions date column; add "93-03-29". Revision level block; change from: "C" to: "D". Rev status of sheets; For sheet 1 change from: "C" to: "D". Rev status of sheets; For sheets 2, 4, 5, 6, 7, and 19 change from: "B" to "D". Sheet 2: Paragraph 1.4, Recommended operating conditions; add: "Input high voltage (V_{IL}) ----- 2.0 V minimum". "Input low voltage (V_{IL}) ----- 0.8 V maximum". Sheet 4: Input high voltage test, Device type column, devices 01-04; add: "3/". Input low voltage test, Device type column, devices 01-04; add: "3/". Sheet 5: Supply current dynamic test, I_{DDU}, Conditions column; change from: "F = 10 MHz" to: "F = 2 MHz". Supply current dynamic test, I_{DDU}, Max limit; change from: "50" to: "10". Supply current dynamic test, I_{DDU}, Conditions column; change from: "F = 22 MHz" to: "F = 20 MHz"; add "<u>3</u>/". Sheet 6: Test column; delete "accumulate" from "Multiply accumulate time". Conditions column; change from: ${}^{"}C_L = 20 \; pF$ " to: ${}^{"}C_L = 20 \; pF$ minimum". Sheet 7: Clock pulse width test, Conditions column; change from: ${}^{"}C_L = 20 \text{ pF}$ " to: ${}^{"}C_L = 20 \text{ pF}$ minimum"; add: ${}^{"}\underline{3}$ /". Output enable test, t_{ENA} , Conditions column; change from: ${}^{"}C_L = 20 \text{ pF}$ " to: ${}^{"}C_L = 20 \text{ pF}$ minimum". Sheet 19: TABLE III; delete line between " X_{7-0} " and " Y_{7-0} ", and between their respective descriptions. Sheets 2, 4, 5, 6, 7, 19: Revision level block; change from: "B" to: "D". 11. THIS SECTION FOR GOVERNMENT USE ONLY a. CHECK ONE [X] EXISTING DOCUMENT SUPPLEMENTED [] REVISED DOCUMENT MUST BE [] CUSTODIAN OF MASTER DOCUMENT BY THIS NOR MAY BE USED IN RECEIVED BEFORE MANUFACTURER SHALL MAKE ABOVE REVISION AND FURNISH REVISED DOCUMENT TO: MANUFACTURE. MAY INCORPORATE THIS CHANGE. b. ACTIVITY AUTHORIZED TO APPROVE SIGNATURE AND TITLE DATE (YYMMDD) CHANGE FOR GOVERNMENT MONICA L. POELKING 93-03-29 **DESC-ECC** Chief. Custom Microelectronics 12. ACTIVITY ACCOMPLISHING REVISION **REVISION COMPLETED (Signature)** DATE (YYMMDD) **DESC-ECC** WANDA L. MEADOWS 93-03-29

NOTICE OF REVISION (NOR)

DATE (YYMMDD)

Form Approved

NOTICE OF REVISION (NOR)

(See MIL-STD-480 for instructions) This revision described below has been authorized for the document listed. 13DATE (YYMMDD) 93 - 09 - 11

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1. ORIGINATOR NAME AND ADDRESS	2. CAGE CODE	3. NOR NO.
Defense Electronics Supply Center	67268	5962-R310-93
Dayton, Ohio 45444-5277	4. CAGE CODE	5. DOCUMENT NO.
	67268	5962-88739
6. TITLE OF DOCUMENT	7. REVISION LETTER	
MICROCIRCUITS, DIGITAL, CMOS, 8 X 8 MULTIPLIER, MONOLITHIC	(Current) B	(New) C
SILICON	8. ECP NO.	

9. CONFIGURATION ITEM (OR SYSTEM) TO WHICH ECP APPLIES

10. DESCRIPTION OF REVISION

Sheet 1: Revisions Itr column; add "C".

Revisions description column; add "Changes in accordance with NOR 5962-R310-92".

Revisions date column; add "92-09-11". Revision level block; change from "B" to "C".

Rev status of sheets 1, 17, and 18; change from "B" to "C".

Sheet 17: Paragraph 4.2.a.1; change from: "Test condition D using the circuit submitted..."

to: "Test conditions A or D using the circuit submitted...".

Sheet 18: Paragraph 4.3.2.b.1; change from: "Test condition D using the circuit submitted..."

to: "Test conditions A or D using the circuit submitted...".

Sheets 17 and 18: Revision level block; change from "B" to "C".

11. THIS SECTION FOR GOVERNMENT USE ONLY

a. CHECK ONE [X] EXISTING DOCUMENT SUPPLEMENTED BY THIS NOR MAY BE USED IN MANUFACTURE.	REVISED DOCUMENT MUST BE RECEIVED BEFORE MANUFACTURER MAY INCORPORATE THIS CHANGE.	[] CUSTODIAN OF MASTER DOCUMENT SHALL MAKE ABOVE REVISION AND FURNISH REVISED DOCUMENT TO:
b. ACTIVITY AUTHORIZED TO APPROVE CHANGE FOR GOVERNMENT DESC-ECC	SIGNATURE AND TITLE MONICA L. POELKING Chief, Custom Microelectronics	DATE (YYMMDD) 93-09-11
12. ACTIVITY ACCOMPLISHING REVISION DESC-ECC	REVISION COMPLETED (Signature) WANDA L. MEADOWS	DATE (YYMMDD) 93-09-11

	1							ı	REVISI	ONS			ı				1			
LTR			DESCRIPTION							DATE	E (YR-MC	D-DA)			APPR	OVED				
А	chip	Changes to 1.2.1. Made technical changes to table I. Added a square chip carrier package to 1.2.2. Changes to figure 1 and figure 4. Added vendor CAGE number 59621 for the square chip carrier package.						91-10-18				Monica L. Poelking								
В	Added device types 05 through 08. Made technical changes to table I. Added CAGE number 65896 for device types 05 through 08. Editorial changes throughout.								06-19		Tim	Noh								
REV				THE	ORIGI	NAL FI	IRST P	AGE O	F THIS	DRAW	ING H	AS BEE	EN REF	PLACE). 					
REV SHEET				THE	ORIGI	NAL FI	IRST P	AGE O	F THIS	DRAW	ING H	AS BEE	EN REF	PLACE	D.					
	В	В	В	THE	ORIGI	NAL FI	IRST P	AGE O	F THIS	DRAW	ING H	AS BEE	EN REF	PLACE	D.					
SHEET REV	B 15	B 16	B 17				RST P	AGE O	F THIS	DRAW	ING H	AS BEE	EN REF	PLACE	D.					
SHEET REV SHEET REV STATU	15 JS			В	B 19	В	B	AGE O	F THIS	DRAW	ING H	AS BEE	EN REF	PLACE	Э.	В	В	В	В	
SHEET REV SHEET	15 JS			B 18	B 19	В										B 10	B 11	B 12	B 13	
SHEET REV SHEET REV STATU OF SHEETS PMIC N/A	15 JS S	16		B 18 REV	B 19	B 20	В	B 2	В	В	B 5	B 6	В 7	B 8	В 9	10	11 PLY C	12	13	
SHEET REV SHEET REV STATU OF SHEETS PMIC N/A STA	15 JS	16		B 18 REV SHE	B 19	B 20	B 1	B 2	В	В	B 5	B 6	В 7	B 8	B 9	10	11 PLY C	12	13	
SHEET REV SHEET REV STATU OF SHEETS PMIC N/A STA MICR DR THIS E AV FOR U	JS S S ANDAF OCIRO RAWIN AILABL	RD CUIT G NG IS .E.		B 18 REV SHE PREP	B 19 / EET	BY PHU	B 1 J NGU'	B 2	В 3	B 4	B 5	B 6	B 7	B 8 CCTRC DAY	B 9 DNICS TON,	SUPF OHIO	11 PLY C 4544	12	13	
SHEET REV SHEET REV STATU OF SHEETS PMIC N/A STA MICR DR THIS E AV FOR U	JS S ANDAF OCIRO RAWIN DRAWIN AILABL JSE BY ARTME ENCIES	RD CUIT G NG IS E ALL NTS OF TH	17 HE	B 18 REV SHE PREP	B 19 / EET ARED	BY PHU Y TIM BY MON	B 1 J NGU'	B 2 YEN H	В 3	B 4	B 5 DE	B 6	B 7	B 8 CCTRC DAY	B 9 DNICS TON,	SUPFOHIO	11 PLY C 4544	12 ENTEI 4	13	

1. SCOPE

- 1.1 <u>Scope</u>. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".
- 1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:



1.2.1 <u>Device type(s)</u>. The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Multiply time
01	TMC208KV	Two's complement 8 x 8 multiplier	70 ns
02 03	TMC208KV1 TMC28KUV	Two's complement 8 x 8 multiplier Unsigned magnitude 8 x 8 multiplier	50 ns 70 ns
04	TMC28KUV1	Unsigned magnitude 8 x 8 multiplier	50 ns
05 06	LMU0860 LMU0845	Two's complement 8 x 8 multiplier Two's complement 8 x 8 multiplier	60 ns 45 ns
07 08	LMU8U60 LMU8U45	Unsigned magnitude 8 x 8 multiplier Unsigned magnitude 8 x 8 multiplier	60 ns 45 ns
00	LIVIO0043	Orisigned magnitude o x o multiplier	40118

1.2.2 Case outline(s). The case outline(s) shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter Case outline

Q	D-5 (40-lead, 2.096" x .620" x .225"), dual-in-line package
X	C-5 (44-lead, .662" x .662" x .120"), leadless chip carrier

1.3 Absolute maximum ratings.

Supply voltage range (V _{DD})
OC voltage applied to outputs
Devices 01,02,03,04
Devices 01,02,03,04
OC input voltage:
Devices 01,02,03,04
Devices 05,06,07,083.0 V dc to +7.0 V dc
Maximum power dissipation <u>1</u> /550 mW
ead temperature (soldering, 10 seconds) +300° C
Thermal resistance, junction-to-case ($^{igotimes}_{ m JC}$) $\dots\dots$ See MIL-M-38510, appendix C
lunction temperature (T _I)
Storage temperature range65°C to +150°C

1.4 Recommended operating conditions.

Supply voltage (V _{DD})
Output high current (I _{OH})2.0 mA maximum
Output low current ()
Output high current (I _{OH}) -2.0 mA maximum Output low current (I _{OL}) Devices 01, 02, 03, 04 4.0 mA maximum
Devices 05, 06, 07, 08 8.0 mA maximum
Case operating temperature range (T _C)55° C to +125° C

 $\underline{1}$ / Must withstand the added P_D due to short circuit test; e.g., I_{OS} .

STANDARD							
MICROCIRCUIT DRAWING							
DEFENSE ELECTRONICS SUPPLY CENTER							
DAYTON, OHIO 45444							

SIZE A		5962-88739
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2. APPLICABLE DOCUMENTS

2.1 <u>Government specification, standard, and bulletin</u>. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510

- Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883

- Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103

- List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

- 3.1 <u>Item requirements</u>. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.
- 3.2 <u>Design, construction, and physical dimensions</u>. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.
- 3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.
- 3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.
- 3.2.3 Input/output data format. The input/output data format shall be as specified on figure 2.
- 3.2.4 Block diagram. The functional block diagram shall be as specified on figure 3.
- 3.3 <u>Electrical performance characteristics</u>. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.
- 3.4 <u>Electrical test requirements</u>. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.
- 3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.7 herein).
- 3.6 <u>Certificate of compliance</u>. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7 herein). The certificate of compliance submitted to DESC-ECC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

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TABLE I. <u>Electrical performance characteristics</u>.

Test	Symbol	Conditions $\underline{1}/$ -55°C \leq T _C \leq +125°C 4.5 V \leq V _{CC} \leq 5.5 V unless otherwise specified		Device types	Group A Subgroups	Li	imits	Unit
				31	3 1	Min	Max	
Output high voltage	V _{OH}	V _{DD} = 4.5 V,	V _{DD} = 4.5 V, I _{OH} = -2.0 mA		1, 2, 3	2.4		V
				05, 06, 07, 08	1, 2, 3	3.5		V
Output low voltage	V _{OL}	V _{CC} = 4.5 V,	I _{OL} = 4.0 mA	01, 02, 03, 04	1, 2, 3		0.4	V
			I _{OL} = 8.0 mA	05, 06, 07, 08	1, 2, 3		0.5	V
Input high voltage	V _{IH}	V _{DD} = 5.5 V		01, 02, 03, 04	1, 2, 3	2.0		V
				05, 06, 07, 08	1, 2, 3	2.0		V
Input low voltage	V _{IL}	V _{DD} = 5.5 V		01, 02, 03, 04	1, 2, 3		0.8	V
				05, 06, 07, 08	1, 2, 3		0.8	V
Input low current	I _{IL}	$V_{DD} = 5.5 \text{ V} $ $V_{IN} = 0 \text{ V}$		01, 02, 03, 04	1, 2, 3		-10	uA
				05, 06, 07, 08	1, 2, 3		-20	uA
Input high current	I _{IH}	$V_{DD} = 5.5 \text{ V}$ $V_{IN} = V_{DD}$		01, 02, 03, 04	1, 2, 3		+10	uA
				05, 06, 07, 08	1, 2, 3		+20	uA

See footnotes at end of table.

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TABLE I. <u>Electrical performance characteristics</u> - Continued.

Test	Symbol	Conditio	ons <u>1</u> / C ≤ +125°C	Device types	Group A Subgroups	Li	mits	Unit
		4.5 V ≤ V	CC ≤ 5.5 V wise specified			Min	Max	
Output leakage current, low	I _{OZL}	$V_{DD} = 5.5 \text{ V},$ $V_{IN} = 0 \text{ V}$		01, 02, 03, 04	1, 2, 3		-40	uA
				05, 06, 07, 08	1, 2, 3		-20	uA
Output leakage current, high	I _{OZH}	$V_{DD} = 5.5 \text{ V},$ $V_{IN} = V_{DD}$		01, 02, 03, 04	1, 2, 3		+40	uA
				05, 06, 07, 08	1, 2, 3		+20	uA
Output chort circuit current	los	V _{DD} = 5.5 V		01, 02, 03, 04	1, 2, 3		-100	mA
<u>2</u> / <u>3</u> /				05, 06, 07, 08	1, 2, 3		-125	mA
Supply current, quiescent	I _{DDQ}	V _{DD} = 5.5 V	V _{IN} = 0 V	01, 02, 03, 04	1, 2, 3		5	mA
			<u>4</u> /	05, 06, 07, 08	1, 2, 3		1.0	mA
Supply current, dynamic	I _{DDU}	V _{DD} = 5.5 V; TRIL= 5.0 V; I	TRIM, F = 10MHz	01, 02, 03, 04	1, 2, 3		50	mA
		V _{DD} = 5.5 V; TRIL= 5.0 V; I	TRIM, F = 22MHz	01, 02, 03, 04	1, 2, 3		100	mA
	I _{DD}	V _{DD} = 5.5 V; TRIM, TRIL =	F= 5 Mhz, 5.0 V	05, 06, 07, 08	1, 2, 3		24	mA
Input capacitance	C _{IH}	f = 1.0 MHz TC = +25° C		All	4		10	pF
Output capacitance	C _{OUT}	See 4.3.1c					10	pF

See footnotes at end of table.

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TABLE I. <u>Electrical performance characteristics</u> - Continued.

Test	Symbol	Conditions <u>1</u> / -55° C ≤ T _C ≤ +125° C	Device types	Group A Subgroups	Li	mits	Unit
		4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	71	0 1	Min	Max	
Functional testing <u>5</u> /		V _{DD} = 4.5 V, 5.5 V See 4.3.1d	All	7, 8			
Multiply accumulate	t _{MPY}	See figure 4 <u>5</u> /	01, 03	9, 10, 11		70	ns
time		$V_{DD} = 4.5 V$ $C_{L} = 20pF$	02, 04	10		50	ns
			05, 07	9, 10, 11		60	ns
			06, 08	9, 10, 11		45	ns
Output delay	t _D		01, 03	9, 10, 11		45	ns
			02, 04	10		30	ns
			05, 06, 07, 08	9, 10, 11		22	ns
Input setup time	t _S		01, 03	9, 10, 11	30		ns
			02, 04	10	25		ns
			05, 06, 07, 08	9, 10, 11	15		ns
Input hold time 3/	t _H		All	9, 10, 11	0		ns
Clock pulse width, high	t _{PWH}		01, 02, 03, 04	9, 10, 11	15		ns
			05, 07	9, 10, 11	20		ns
			06, 08	9, 10, 11	15		ns

See footnotes at end of table.

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TABLE I. <u>Electrical performance characteristics</u> - Continued.

Test	Symbol	Conditions <u>1</u> / -55° C ≤ T _C ≤ +125° C	Device types	Group A Subgroups	Li	Unit	
		$4.5 \text{ V} \leq \overrightarrow{V_{CC}} \leq 5.5 \text{ V}$ unless otherwise specified		5 1	Min	Max	
Clock pulse width, low	t _{PWL}	Not shown <u>5</u> / V _{DD} = 4.5 V	01, 02, 03, 04	9, 10, 11	15		ns
		$C_L = 20 \text{ pF}$	05, 07	9, 10,11	20		ns
			06, 08	9, 10, 11	15		ns
Three-state output	t _{ENA}	See figure 4 <u>5</u> /	01, 03	9, 10, 11		45	ns
enable time		V _{DD} = 4.5 V C _L = 20 pF	02, 04	10		25	ns
			05, 06, 07, 08	9, 10, 11		24	ns
Three-state output			01, 03	9, 10, 11		45	ns
disable time	^t DIS		02, 04	10		25	ns
			05, 06, 07, 08	9, 10, 11		22	ns

- $\underline{1}/$ Unless otherwise specified, all testing shall be conducted under worst-case conditions.
- 2/ One output to ground, 1 second duration maximum, output high.
- $\underline{3}$ / Guaranteed, if not tested, to the specified limits.
- $\underline{4}/\;$ Tested with all inputs within 0.1 V of $V_{\mbox{\scriptsize DD}}$ or ground, no load.
- $\underline{\textbf{5}}/\;$ All transitions are measured at a 1.5 V level except $t_{\mbox{DIS}}$ and $t_{\mbox{ENA}}.$

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Devic	e type	All								
Case	outline	Q								
Terminal number	Terminal symbol	Terminal number	Terminal symbol		Terminal number	Terminal symbol		Terminal number	Terminal symbol	
1	P ₁₀	11	P ₃		21	X ₆		31	Y ₄	
2	P ₉	12	P ₂		22	X ₇		32	GND	
3	P ₈	13	P ₁		23	CLK X		33	Y ₅	
4	CLK P	14	P ₀		24	CLK Y		34	Y ₆	
5	TRIM	15	X_0		25	RND		35	Y ₇	
6	TRIL	16	X ₁		26	Y ₀		36	P ₁₅	
7	P ₇	17	X ₂		27	Y ₁		37	P ₁₄	
8	P ₆	18	X ₃		28	Y ₂		38	P ₁₃	
9	P ₅	19	X ₄		29	Y ₃		39	P ₁₂	
10	P ₄	20	X ₅		30	V _{DD}		40	P ₁₁	

FIGURE 1 <u>Terminal connections</u>.

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Devic	e type	All								
Case	outline	X								
Terminal number	Terminal symbol	Terminal number	Terminal symbol		Terminal number	Terminal symbol		Terminal number	Terminal symbol	
1	P ₁₀	12	P ₃		23	X ₆		34	Y ₄	
2	P ₉	13	P ₂		24	X ₇		35	GND	
3	P ₁₀	14	P ₁		25	CLK X		36	Y ₅	
4	P ₈	15	P_0		26	CLK Y		37	Y ₆	
5	CLK P	16	X ₀		27	RND		38	Y ₇	
6	NC	17	NC		28	NC		39	NC	
7	TRIM	18	X ₁		29	Y ₀		40	P ₁₅	
8	P ₇	19	X ₂		30	Y ₁		41	P ₁₄	
9	P ₆	20	X ₃		31	Y ₂		42	P ₁₃	
10	P ₅	21	X_4		32	Y ₃		43	P ₁₂	
11	P ₄	22	X ₅		33	V _{DD}		44	P ₁₁	

FIGURE 1 <u>Terminal connections</u> - Continued.

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Device types 01, 02, 05, and 06 Fractional two's compliment notation Binary point Signal X₇ X_0 X₅ X_4 X_2 -2⁰ 2-7 Digit value Y₆ Y₇ Y₅ Y3 Signal Y_4 Y₂ Y_0 -2⁰ 2-6 2-2 2-5 2-7 Digit value P₈ P₉ P₁ P₇ P₆ P₅ P_4 P_3 P_2 P_0 Signal 3 0 2-2 2⁻⁶ 2-9 2-3 2-4 2-5 2-7 ₋₂-0 2⁻⁸ 2-10 2-11 2-12 2-13 2-14 2-1 -2⁰ Digit value MSP LSP

FIGURE 2. Input.output data format.

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Device types 01, 02, 05, and 06 Integer two's complement notation Binary point X₅ X₁ x_3 Χ X_4 X₂ Signal X₇ X_0 20 ₋₂7 26 25 24 23 22 21 Digit value Y_4 Y_2 Υ Y₁ Signal Y₇ Y₅ Y₃ Y_0 25 ₂6 ₋₂7 2^4 23 22 21 20 Digit value P₁ P₈ P_4 P_2 P₁ P₁₅ P₁ P₉ P₅ P_0 Singal P₇ P_3 6 3 0 2¹ -214 2¹ 29 28 26 2⁵ 23 22 27 24 21 20 Digit value 214 MSP LSP FIGURE 2. <u>Input.output data format</u> - Continued. SIZE 5962-88739 **STANDARD** Α MICROCIRCUIT DRAWING **DEFENSE ELECTRONICS SUPPLY CENTER** REVISION LEVEL SHEET **DAYTON, OHIO 45444** 11

Device types 03, 04, 07, and 08 Fractional unsigned magnitude notation Binary point Signal Digital value Signal Χ 2-5 2-6 2-7 2-8 2-3 2-2 Digital value P₈ P₁ P₁ P₉ P₆ P_5 P_4 P_3 P_2 P₁ P_0 Signal 2-2 2-5 2-9 2-3 2-6 2-8 2-1 2-7 2⁻ 10 2<u>-</u> 11 2<u>-</u> 14 2⁻ 15 2⁻ 16 2<u>-</u> 12 2<u>-</u> 13 Digital value MSP LSP

FIGURE 2. Input.output data format - Continued.

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Device types 03, 04, 07, and 08 Integer unsigned magnitude notation Binary point Y_0 Signal Y₇ ^Y6 Y₅ Υ₄ Y₃ Y₂ Y₁ 27 26 25 24 23 22 21 20 Digital value Signal ^Y6 Y₅ Y_4 Y_3 Y_2 Y₁ Y_0 Χ 27 24 22 21 26 25 23 20 Digital value P₁ P_1 P_9 P₈ P_6 P_5 P_4 P_3 P_2 P_1 P_0 Signal 5 21 21 21 21 21 210 29 28 27 26 25 24 23 22 21 20 Digital value 5 2 LSP MSP SIZE **STANDARD** 5962-88739 Α MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER SHEET REVISION LEVEL **DAYTON, OHIO 45444** 13

FIGURE 2. Input.output data format - Continued.			
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Device types 01, 02, 05, and 06

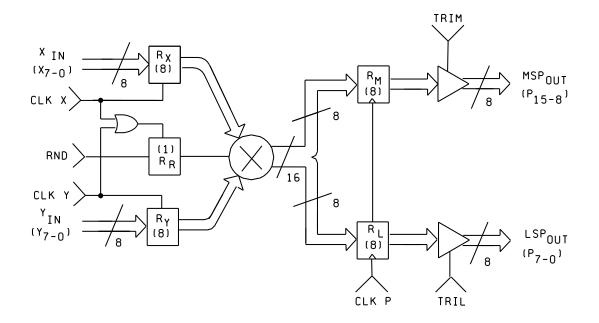


FIGURE 3. Block diagram.

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Device types 03, 04, 07, and 08

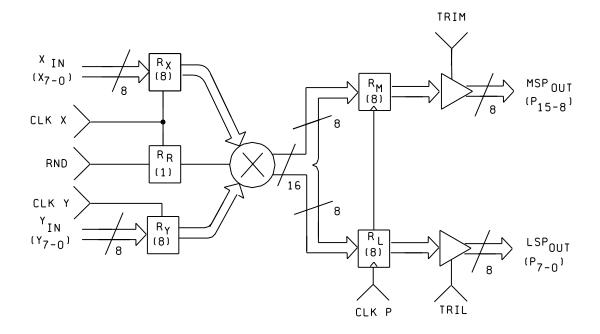
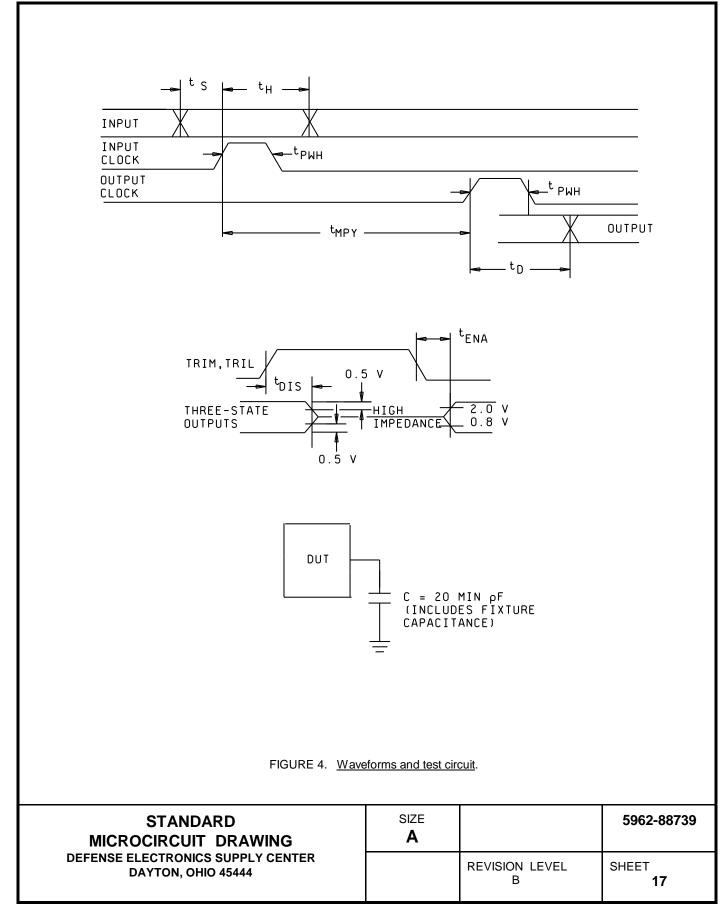


FIGURE 3. <u>Block diagram</u> - Continued.

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- 3.7 <u>Certificate of conformance</u>. A certificate of conformance as required in MIL-STD-883 (see 3.1herein) shall be provided with each lot of microcircuits delivered to this drawing.
- 3.8 <u>Notification of change</u>. Notification of change to DESC-ECC shall be required in accordance with MIL-STD-883 (see 3.1 herein).
- 3.9 <u>Verification and review</u>. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.
- 4. QUALITY ASSURANCE PROVISIONS
- 4.1 <u>Sampling and inspection</u>. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).
- 4.2 <u>Screening</u>. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:
 - a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition D using the circuit submitted with the certificate of compliance (see 3.6 herein).
 - (2) $T_A = +125^{\circ} C$, minimum.
 - b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per mehtod 5005, table 1)
Interim electrical parameters (method 5004)	
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C and D end-point electrical parameters (method 5005)	1, 2, 7, 9

^{*} PDA applies to subgroups 1 and 7.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

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4.3.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample size of five devices with zero rejects shall be required.
- d. Subgroups 7 and 8 shall consist of verifying the functionality of the device.

4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
 - (1) Test condition D using the circuit submitted with the certificate of compliance (see 3.6 herein).
 - (2) $T_A = +125^{\circ} C$, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

- 6.1 <u>Intended use</u>. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.
- 6.2 <u>Replaceability</u>. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.
- 6.3 <u>Configuration control of SMD's</u>. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).
- 6.4 <u>Record of users</u>. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECC, telephone (513) 296-8526.
- 6.5 Pin descriptions. See table III.
- 6.6 <u>Comments</u>. Comments on this drawing should be directed to DESC-ECC, Dayton, Ohio 45444, or telephone (513) 296-8526.
- 6.7 <u>Approved sources of supply</u>. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECC.

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TABLE III. Pin description.

Pin	Description
V _{DD,} GND	The devices operate from a single +5 volt supply. All power and ground lines must be connected.
X ₇₋₀	Devices 01, 02, 05, and 06 have two 8-bit two's complement data inputs labeled X and Y.
Y ₇₋₀	Devices 03, 04, 07, and 08 have two 8-bit unsigned magnitude data inputs labeled X and Y. The most significant bits (MSB's) X_7 and Y_7 , carry the sign information for the two's complement notation in devices 01, 02, 05, and 06. The remaining bits are X_{6-0} and Y_{6-0} with X_0 and Y_0 the LSB's. The input and output formats for fractional and integer two's complement, and fractional and integer unsigned magnitude notations are shown on figure 2.
P ₁₅₋₀	Devices 01, 02, 05, and 06 have a 16-bit two's complement output which is the product of the two input X and Y values. Devices 03, 04, 07, and 08 have a 16-bit unsigned magnitude output which is the product of the two input X and Y values. This output is divided into two 8-bit output words, the MSP and LSP. The MSB both the MSP and LSP is the sign bit in devices 01, 02, 05, and 06. The input and output formats for fractional and integer two's complement, and fractional and integer unsigned magnitude notations are shown on figure 2. Note that since +1 cannot be exactly represented in fractional two's complement notation, some provision for handling the case (-1)*(-1) must be made. Devices 01, 02, 05, and 6 output a -1 in this case. As a result, external error handling provisions may be required.
CLK X, CLK Y CLK P	These devices have three clock lines, one for each input register (CLK X and CLK Y) and one for the product register (CLK P). Data present at the inputs of these CLK P registers are loaded into the registers on the rising edge of the appropriate clock. In devices 01, 02, 05, and 06, the RND input is registered and clocked in on the rising edge of the logical OR of both CLK X and CLK Y. Special attention to the clock signals is required if normally high clock signals are used. Problems with loading this control signal can be avoided by the use of normally low clocks. In devices 03, 04, 07, and 08, the RND input is registered and clocked in on the rising edge of CLK X.
TRIM, TRIL	TRIM and TRIL are the three-state enable lines for the MSP and the LSP. The output TRIL driver is in the high impedance state when TRIM or TRIL is high, and enabled when low. TRIM and TRIL are not registered.
RND	When RND (round) is high, one is added to the MSB of the LSP. A one will be added to the P_6 bit in devices 01, 02, 05, and 06, or the P_7 bit in devices 03, 04, 07, and 08. Note that rounding always occurs in the positive direction. In some applications, this may introduce a systematic bias. The RND input is registered and used when a rounded 8-bit product is desired.

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STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 92-06-19

Approved sources of supply for SMD 5962-88726 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-ECS. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar part number <u>1</u> /
5962-8873901QX	59621	TMC208KB5V
5962-8873901XX	59621	TMC208KC2V
5962-8873902QX	59621	TMC208KB5V1
5962-8873902XX	59621	TMC208KC2V1
5962-8873903QX	59621	TMC28KUB5V
5962-8873903XX	59621	TMC28KUC2V
5962-8873904QX	59621	TMC28KUB5V1
5962-8873904XX	59621	TMC28KUC2V1
5962-8873905QX	65896	LMU08DMB60
5962-8873905XC	65896	LMU08KMB60
5962-8873906QX	65896	LMU08DMB45
5962-8873906XX	65896	LMU08KMB45
5962-8873907QX	65896	LMU8UDMB60
5962-8873907XX	65896	LMU8UKMB60
5962-8873908QX	65896	LMU8UDMB45
5962-8873908XX	65896	LMU8UKMB45

1 / Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE <u>number</u>	Vendor name <u>and address</u>
59621	TRW LSI Products, Incorporated 4243 Campus Point Court San Diego, CA 92121
65896	Logic Devices, Incorporated 628 E. Evelyn Avenue Sunnyvale, CA 94086

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